Wafer Processing Capabilities

silex MICROSYSTEMS

Silex Microsystems is a leader in pure-play MEMS manufacturing, offering Class 1-10, 200mm (8-inch) fabs, with state-of-the-art equipment and new capabilities. Committed to meeting customers' expectations today and into the future, Silex provides the industry's most advanced process technology development combined with proven manufacturing experience. In addition, Silex offers cutting edge standard technology blocks, solving some of the most difficult industry challenges such as through-wafer connections (Sil-Via®), low temperature wafer-level bonding and integration of piezo electric materials. Integrating state-of-the-art deposition and electroplating equipment, Silex is able to implement novel functional capping technologies with through-wafer metal vias, RF passives and coaxial feedthroughs. Silex' advanced wafer-level packaging technologies are spearheading the MEMS industry when it comes to integration of CMOS with MEMS.

Lithography	
Contact 1:1 Aligner:	Front/Back Side
Alignment Accuracy:	~1.0µm, Front Side ~2.0µm, Back Side
Minimum Features:	~0.8µm, vacuum mode ~3.0µm, proximity mode
Stepper 5:1 Aligner:	Front/Back Side
Alignment Accuracy:	~0.1µm
Minimum Features:	~0.35µm
Resist Thicknesses:	1-10µm, Positive 1-10µm, Negative
BCB, Polyimide, Epoxy-Based Materials	
Lift-Off	
Spray Coating for Patterning in Recesses	
Dry Film Processing	

Plasma Etching
DRIE with high selectivity and 1:50 feature aspect ratio
Dielectric Etching (SiO2, SiN, etc.), Polysilicon Etching
Polymer Etching and Stripping
Metals

Plasma Deposition
PECVD Oxide, PECVD Nitride, PECVD TEOS
SACVD Oxide

Wafer Bonding
Silicon Fusion Bonding
Au-Si, Au-Sn Eutectic Bonding
Anodic Bonding
Thermo-compression Bonding
Adhesive Bonding
Alignment Accuracy: Wafer Pairs, <3.0µm
Multi-wafer Stacks: <5.0µm
DI Wafer Clean (Megasonic; Brush)
Controlled Ambient or Vacuum

Metallization
Sputter Deposition
Electroplating and Electroless plating
Evaporation

Technology Blocks
Via Technologies (Sil-Via®, Met-Via®, TGV)
Wafer Level Packaging (WLP)

Materials
PZT, AlN, Ge, Ta, Pt, Ti, TiW, TiN, Ti/TiO/Pt, Au, Sn, AuSn, Al, Cu, Ni, Cr, NiCr, Ag, Mo, IPD & Ferro-Magnetic

Other Capabilities
(ALD) Atomic Layer Deposition
(CMP) Chemical Mechanical Planarization

Furnace Process	
Thermal Oxidations: (900-1050°C)	Wet/Dry/Mixed
Annealing Processes (densification, bond or forming gas)	
Vacuum Anneal	
Metal Sintering	
RTP	
Doping Processes (ion implantation)	
LPCVD nitride (including low stress)	
LPCVD oxides (LTO, PSG, TEOS)	
LPCVD Silicon (including IDP)	

Wet Etching
Anisotropic silicon etching (KOH, TMAH)
Wet etching of dielectrics (i.e. different oxides and nitrides)
Isotropic etching of glass
Wet cleaning process (acid and solvent based)
Fully-automated Spin Solvent
Fully-automated Spin Acid

Metrology
SEM with CD-Tool and FIB-SEM
Ellipsometer
Interferometer
Inspection Microscopes
CD Microscopes
White Light Interferometer
Surface Profiler
Film Stress Measurement
Sheet Resistance (4-point probe)
Surfscan
xRD

Testing
Automated Optical Inspection
Automatic Wafer Scale Testing
Customer-specific Test Rigs
Test Development (Prototyping and Volume Production)

Back End
Automated Dicing
Stealth Dicing
Lapping for Wafer Thinning and Polishing
Epoxy and Solder Die Attach

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